Customer No.: 31561
Docket No.: 09946-US-PA-1
Application No.: 10/711,004

AMENDMENT

Please amend the application as indicated hereaftter.

In the Claims:

1. (currently amended) A read only memory device with a high dielectric constant tunneling dielectric layer, comprising:

a substrate;

a tunneling dielectric layer, disposed over the substrate, wherein the tunneling dielectric layer is formed with a material selected from the group consisting of HfSiON and HfO_xN_y, wherein the tunneling dielectric layer reduces leakage of electrons stored in the charge trapping layer into the substrate;

an electron trapping layer, disposed over the tunneling dielectric layer;

a top ~~oxide~~ dielectric layer, disposed over the electron trapping layer, wherein the tunneling dielectric layer, the electron trapping layer and the top ~~oxide~~ dielectric layer form a stacked structure;

a conductive layer, disposed at least over the top ~~oxide~~ dielectric layer; and

a buried ~~drain~~ diffusion region, configured in the substrate beside both sides of the stacked structure.

2. (original) The read only memory device with a high dielectric constant tunneling dielectric layer of claim 1, wherein a dielectric constant of the tunneling dielectric layer is greater than a dielectric constant of silicon dioxide.

3. (currently amended) The read only memory device with a high dielectric constant tunneling dielectric layer of claim 1, wherein a buried drain oxide layer is further disposed over the buried ~~drain~~ diffusion region beside both sides of the stacked structures.

4. (original) The read only memory device with a high dielectric constant tunneling dielectric layer of claim 1, wherein the electron trapping layer comprises silicon nitride.

Claim 5 (canceled).

6. (new) A read only memory device with a high dielectric constant tunneling dielectric layer, comprising:

a substrate;

an electron trapping layer, disposed over the tunneling dielectric layer;

a tunneling dielectric layer, disposed between the substrate and the electron trapping layer, wherein the tunneling dielectric layer is formed with a material selected from the group consisting of HfSiON, HfO_xN_y, ZrO_2, HfO_2 and ZrO_xN_y, wherein the tunneling dielectric layer reduces leakage of electrons stored in the charge trapping layer into the substrate;

a top dielectric layer, disposed over the electron trapping layer, wherein the tunneling dielectric layer, the electron trapping layer and the dielectric layer form a stacked structure;

a conductive layer, disposed over the top dielectric layer; and

a buried diffusion region, configured in the substrate beside both sides of the stacked structure.

7. (new) The read only memory device with a high dielectric constant tunneling dielectric layer of claim 6, wherein a dielectric constant of the tunneling dielectric layer is greater than a dielectric constant of silicon dioxide.

8. (new) The read only memory device with a high dielectric constant tunneling dielectric layer of claim 6, wherein a buried drain oxide layer is further disposed over the buried diffusion region beside both sides of the stacked structures.

9. (new) The read only memory device with a high dielectric constant tunneling dielectric layer of claim 6, wherein the top dielectric layer comprises silicon oxide.

10. (new) The read only memory device with a high dielectric constant tunneling dielectric layer of claim 1, wherein the top dielectric layer comprises silicon oxide.